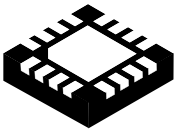
STCC5011, STCC5021

USB charging controller with integrated power switch and attach detector

Datasheet - production data



VFQFPN 16L - 3 x 3 x 0.8 mm

Applications

- USB ports/hubs
- Personal computers, all-in-one PCs
- Monitors
- Notebooks, ultrabooks
- Tablet PCs
- Universal wall charging adapters

Features

- Compliant with USB charging specifications BC1.2, USB 2.0 and USB 3.0 standards
- Compliant with Chinese telecommunications industry standard YD/T 1591-2009
- Compatible with proprietary charging mode (Apple® 1 A / 2 A, BlackBerry®, Korean tablets)
- Wide bandwidth, low-loss USB 2.0 data switch
- Integrated V_{BUS} power switch with low R_{ON} of 65 mΩ
- Constant current mode overcurrent protection
- Soft-start to limit inrush current
- Adjustable current limit up to 2.8 A
- Short-circuit, thermal and undervoltage protection
- Reverse voltage and reverse current protection
- Deglitched fault reporting output
- Supports remote wakeup in S3
- Charging indication output in DCP and CDP modes
- 3-hour safety counter for charging in S5
- Device attachment detection in G3 state
- Available in VFQFPN 16L 3 x 3 x 0.8 mm package with exposed pad
- Temperature range: -40 up to 85 °C
- UL and CB recognized components (UL file number: E354278)

Description

The STCC5011/STCC5021 device integrates, in one package, a USB charger controller, a wide bandwidth data switch and a high current power switch. The device emulates several profiles compatible with the USB battery charging standard BC1.2, Chinese telecommunications standard YD/T 1591-2009 and proprietary charger modes.

The device can detect peripheral device attachment when the host is in S4/S5 deep sleep/off states or in G3 shutdown state. It asserts the $\overline{\text{CHARGING/ATTACH}}$ output after the attach event, allowing the host to turn on the high power DC-DC converter and start charging.

This device also asserts the $\overline{\text{CHARGING/ATTACH}}$ output in DCP modes if the charging current is above the threshold. In CDP mode, it asserts the $\overline{\text{CHARGING/ATTACH}}$ output after the CDP negotiation if the charging current is above the threshold.

After the current drops below the threshold, the output is deasserted. This allows the host to turn off the high power DC-DC converter and reduce overall consumption in S4/S5 or in G3 states which is critical when the host is battery-supplied.

These two features permit the host system to reduce consumption while no device is attached or when there is no charging.

This is information on a product in full production. www.st.com

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1 Functional description

The STCC5011 and STCC5021 devices integrate, in one package, a complete solution to charge portable devices through USB ports. Functions include:

- Charger emulator compatible with USB battery charging BC1.2 standard, Chinese telecommunications standard YD/T 1591-2009 and proprietary chargers such as Apple® divider mode, BlackBerry® and Korean tablet charging mode.
- The Apple divider mode comes in 2 profiles:
  - 1 A max. current drawn: for Apple iPod®, iPhone® (STCC5011)
  - 2 A max. current drawn: for Apple iPad®, supporting also Apple iPod and iPhone (STCC5021)
- 3 control pins, CTL1, CTL2, CTL3 allowing the host to select the emulation profile. These pins may be controlled directly from the host USB controller or from the embedded controller.
- USB data switch with wide bandwidth up to 1100 MHz compliant with USB 2.0 standard. This wide bandwidth switch features low capacitance and low R_{ON} resistance, allowing signals to pass with minimum edge and phase distortion.
- N-channel power switch with low R_{ON} resistance of 65 mΩ typ., high current limiter accuracy and high current output capability, 2.5 A typ. The current limit threshold can be adjusted with a good accuracy by an external resistor in the range 500 mA to 2.8 A. Constant current mode protection is used to protect the device and the host system against overcurrent or short-circuit. Other protection includes reverse current and reverse voltage protection, undervoltage lockout and thermal shutdown.
- A deglitched output ($\overline{FAULT}$) reporting the failure events of overcurrent, thermal shutdown and reverse current (backdrive) to V_{IN}.
- Charging current sensing circuit. The output $\overline{CHARGING}/\overline{ATTACH}$ is asserted if charging current is above 20 mA in CDP and DCP modes.
  In CDP mode the charging flag is asserted only if the CDP handshaking between the portable device and the host is performed before the current is above the threshold.
  Moreover, in S4/S5 power states and battery supplied, there is an additional safety timer to stop the charging process when the “end of charge” timeout is reached. This timer is started only after a device attachment event and can be disabled by toggling the pin ATTACH_EN to low if the timer is not wanted.
  If the timeout or current is below the threshold, the signal $\overline{CHARGING}/\overline{ATTACH}$ is deasserted: in both cases, the host system can disable the high power DC-DC converter and therefore reduce power consumption. This is crucial when the host is battery supplied.
- Attach detector circuit to monitor device attachment.
  This circuit is enabled by driving the ATTACH_EN pin high and EN low. When a device attachment is detected, the output $\overline{CHARGING}/\overline{ATTACH}$ is asserted for a t_{ATTACH} period (25 s typ.). The attach detection block is supplied by the V_{DD} power supply pin.
- An enable input (EN) to enable/disable the device, except the attach detection switch which is also managed by the ATTACH_EN input.

The device is offered in a small, RoHS-compliant VFQFPN 16L (3 x 3 x 0.8 mm) package with an exposed pad for effective cooling.

Figure 1. Block diagram

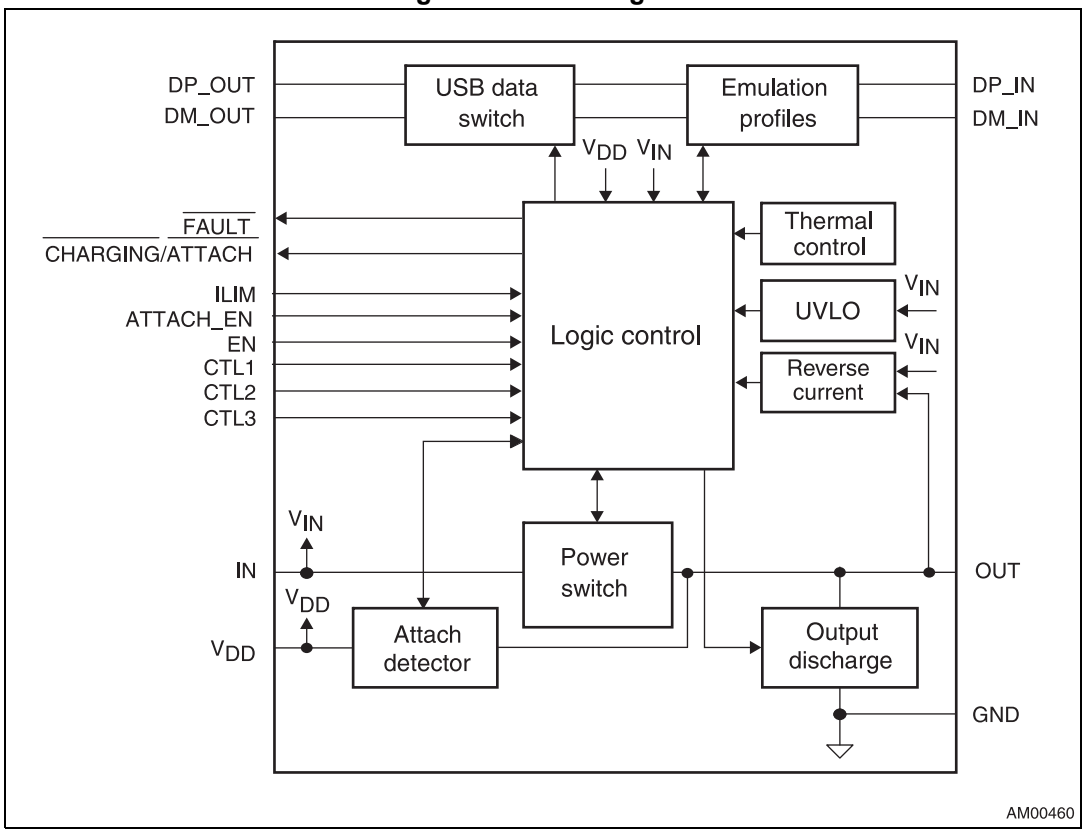
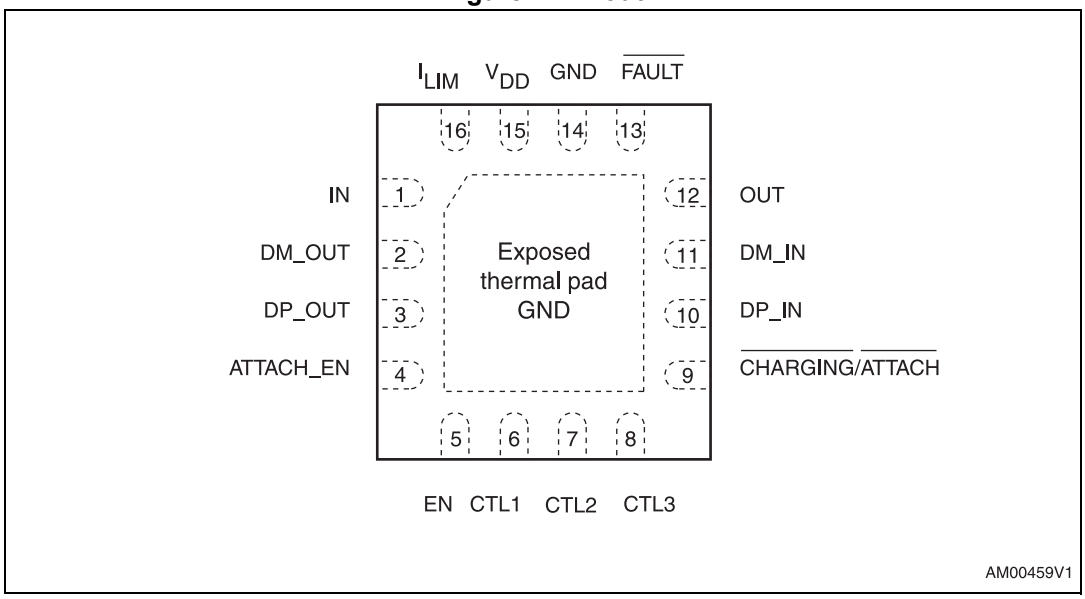


Figure 2. Pinout



2 Pin description

Table 1. Pin description

Pin no.	Name	Type	Description
1	IN	PWR	Device and USB port power supply input
2, 3	DM_OUT, DP_OUT	I/O	USB 2.0 data connection to system USB transmitter (DM = D-, DP = D+)
4	ATTACH_EN	I	Logic level control input to turn on/off the attach detector (see *Table 6*). It can also disable (logic low) the 3-hour timer if started.
5	EN	I	Logic level control input. When EN is low, power switch, data switch and emulator are OFF.
6, 7, 8	CTL1, CTL2, CTL3	I	Logic level control inputs to select charger mode (see *Table 5*).
9	$\overline{\text{CHARGING}}$/$\overline{\text{ATTACH}}$	O	Active low open drain output, asserted when device attachment or charging current is detected.
10, 11	DP_IN, DM_IN	I/O	USB 2.0 data connection to system USB connector (DM = D-, DP = D+)
12	OUT	PWR	USB port power supply output (V_{BUS})
13	$\overline{\text{FAULT}}$	O	Active low open drain output, asserted when overcurrent, overtemperature or reverse voltage are detected.
14	GND	-	Ground
15	V_{DD}	PWR	Attach detector power supply. V_{DD} must **always** be supplied before V_{IN}.
16	I_{LIM}	I	Current limit threshold programming resistor terminal

3 Absolute maximum ratings and operating conditions

Stressing the device beyond the rating listed in *Table 2: Absolute maximum ratings (AMR)* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in *Table 3: Operating conditions* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{IN}, V_{DD}, V_{OUT}	Supply voltage	-0.3 to 6.5	V
V_{EN}, V_{ATTACH_EN}, V_{CTLx}	Logical input voltage		
$V_{\overline{FAULT}}$, $V_{\overline{CHARGING/ATTACH}}$	Pull-up resistor voltage ($\overline{FAULT}$, $\overline{CHARGING}/\overline{ATTACH}$)		
V_{DP_OUT}, V_{DM_OUT}, V_{DP_IN}, V_{DM_IN}	Data switch pin voltage to ground	-0.3 to V_{IN} +0.3	V
I_{DP_OUT}, I_{DM_OUT}, I_{DP_IN}, I_{DM_IN}	Data switch current, switch ON	±50	mA
$I_{O(OUT)}$	Maximum power switch output current, power switch ON	Internally limited	A
$I_{O(\overline{FAULT})}$, $I_{O(\overline{CHARGING/ATTACH})}$	Logical output sink current	25	mA
T_{STG}	Storage temperature (V_{IN} OFF, V_{DD} OFF)	-55 to +150	°C
T_{SLD}	Lead solder temperature for 10 second temperature (V_{IN} OFF, V_{DD} OFF)(1)	260	
R_{thja}	Thermal resistance junction-to-ambient VFQFPN 16L(2)	60	°C/W
T_j	Maximum junction temperature range (internally limited)	-40 to T_{STOP}	°C
$V_{ESD(OUT, DP_IN, DM_IN)}$	IEC61000-4-2 contact discharge (OUT, DP_IN, DM_IN pins)(3)	8	kV
V_{ESD}	JEDEC human body model (all pins)	2	
	JEDEC machine model (all pins)	200	V

1. Reflow at temperatures of 255 °C to 260 °C for time < 30 seconds (total thermal budget not to exceed 180 °C for a period from 90 to 150 seconds).
2. R_{th} are typical values, given when mounted on a 4-layer PCB with vias.
3. Measured in a recommended application circuit with a 1 µF ceramic capacitor + 150 µF low ESR electrolytic capacitor connected between OUT and GND pins (see *Figure 4*).

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{IN}	Supply voltage	4.5 to 5.5	V
V_{DD}	Supply voltage	1.7 to 5.5	
T_A	Ambient operating temperature	-40 to +85	°C
T_J	Junction operating temperature	-40 to +125	

4 Electrical characteristics

Table 4. Electrical characteristics V_{IN} = 4.5 V to 5.5 V, V_{DD} = 1.7 V to 5.5 V, -40 °C < T_J < 125 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Current consumption (V_{IN} domain)						
$I_{IN(ACTIVE)}$	Supply current in active state (EN = 1)	Mode CDP (111)		110	160	µA
		Mode SDP (110 - 010)		100	150	
		Mode DCP auto-detect (001) – Divider mode – BC1.2		 260 110	 290 180	
		Mode DCP BC1.2 (100)		110	180	
		Mode DCP divider (101)		210	290	
$I_{IN(DISABLED)}$	Supply current in disable state (EN = 0)	CTLx <> 000, OUT floating		0.1	5	µA
		CTLx = 000 or OUT grounded, T_J = 25 °C		0.2	5	
		T_J = 125 °C			60	
Power switch - DC parameters						
R_{ON}	Static on-resistance	T_J = 25 °C		65		mΩ
		-40 °C < T_J < 125 °C			95	
$\lvert I_{REVERSE} \rvert$	Reverse leakage current in disabled state (absolute value)	V_{OUT} = 5.5 V, V_{IN} = 0, T_J = 25 °C, V_{EN} = 0, measured at IN		1	5	µA
		T_J = 125 °C, other conditions the same as above			70	
$V_{REVERSE}$	Reverse voltage protection threshold (V_{OUT} - V_{IN})	V_{UVLO} < V_{IN} < V_{OUT}, EN = 1, power switch ON -> OFF		60		mV
I_{OS}	Current limiter threshold	R_{ILIM} = 96 kΩ	340	500	625	mA
		R_{ILIM} = 33 kΩ	1290	1450	1595	
		R_{ILIM} = 19.6 kΩ	2255	2450	2645	
		R_{ILIM} = 17.2 kΩ		2800		
T_{STOP}	Emergency OFF temperature		140	150	160	°C
T_{HYST}	Thermal shutdown hysteresis			20		
R_{EN}	EN input pull-down resistor			250		kΩ
V_{EN}	Enable input turn-on, turn-off threshold voltage		0.4		1.6	V
$V_{HYST(EN)}$	Enable input turn-on, turn-off voltage hysteresis			500		mV
$V_{OL(\overline{FAULT})}$	$\overline{FAULT}$ output low voltage	$I_{\overline{FAULT}}$ = 1 mA			180	

Table 4. Electrical characteristics V_{IN} = 4.5 V to 5.5 V, V_{DD} = 1.7 V to 5.5 V, -40 °C < T_J < 125 °C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{OL(\overline{FAULT})}$	$\overline{FAULT}$ output leakage current	V_{IN} = 5.5 V, V_{DD} = 5.5 V, $V_{\overline{FAULT}}$ = 5 V			1	µA
$t_{\overline{FAULT}}$	$\overline{FAULT}$ output deglitch delay	$\overline{FAULT}$ assertion / deassertion delay in overcurrent condition	7	9	12	ms
V_{UVLO}	Undervoltage lockout	V_{IN} rising	3.9	4.1	4.3	V
$V_{HYST(UVLO)}$	Undervoltage lockout hysteresis	T_J = 25 °C		100		mV
Power switch - AC parameters(1)						
t_{ON}	Turn-on, EN to OUT delay	C_{LOAD} = 1 µF, R_{LOAD} = 100 Ω		0.8		ms
t_{OFF}	Turn-off, EN to OUT delay			0.3		
t_R	OUT (V_{BUS}) rise time	C_{LOAD} = 1 µF, R_{LOAD} = 100 Ω		0.4		
t_F	OUT (V_{BUS}) fall time	C_{LOAD} = 1 µF, R_{LOAD} = 100 Ω		0.2		
t_{IOS}	Current limiter response time to short-circuit	V_{IN} = 5.5 V		3.5		µs
Output discharge						
$R_{DISCHARGE}$	Discharge resistor	ATTACH_EN = EN = 0	140	200	300	Ω
Attach detector						
V_{DD}	Supply voltage		1.7		5.5	V
$I_{DD(ACTIVE)}$	Supply current in active state	V_{DD} = 1.7 V to 5.5 V, V_{EN} = 0, V_{ATTACH_EN} = V_{DD}, T_J = 25 °C		15	30	µA
$I_{DD(DISABLED)}$	Supply current in disabled state	V_{DD} = 1.7 to 5.5 V, V_{EN} = 0, V_{ATTACH_EN} = 0		0.1	3	
$\lvert I_{ATT_REVERSE} \rvert$	Detector switch reverse current (V_{OUT} to V_{DD}) (absolute value)	V_{DD} = 0, V_{OUT} = 5.5 V, IN floating, measured at V_{DD}		0.1	3	
R_{ON_ATT}	Static on-resistance V_{DD} to V_{OUT}	T_J = 25 °C		100		Ω
V_{ATTACH_EN}	Enable input turn-on, turn-off threshold voltage		0.4		1.6	V
$V_{HYST(ATTACH_EN)}$	Enable input threshold hysteresis			500		mV
I_{ATTACH_EN}	ATTACH_EN input leakage current	V_{DD} = 5.5 V, V_{IN} = 5.5 V, V_{ATTACH_EN} = 0 V or 5 V	-1		1	µA
$V_{OL(\overline{CHARGING}/\overline{ATTACH})}$	$\overline{CHARGING}/\overline{ATTACH}$ output low voltage	Device attachment detected, $I_{\overline{CHARGING}/\overline{ATTACH}}$ = 1 mA			180	mV
$I_{OL(\overline{CHARGING}/\overline{ATTACH})}$	$\overline{CHARGING}/\overline{ATTACH}$ output leakage current	V_{IN} = 5.5 V, V_{DD} = 5.5 V, $V_{\overline{CHARGING/ATTACH}}$ = 5 V			1	µA

Table 4. Electrical characteristics V_{IN} = 4.5 V to 5.5 V, V_{DD} = 1.7 V to 5.5 V, -40 °C < T_J < 125 °C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ATTACH}	$\overline{CHARGING}/\overline{ATTACH}$ assertion time after attach detected			25		s
High-speed data switch - DC parameters						
R_{ON}	Data switch on-resistance	Switch closed, V_{IN} = 5 V, I_S = 8 mA, test voltage on DP_OUT, DM_OUT = 0.4 V		2.5	4	Ω
R_{ON}	Data switch on-resistance	Switch closed, V_{IN} = 5 V, I_S = 8 mA, test voltage on DP_OUT, DM_OUT = 3 V		2.7	4	
I_{OFF}	OFF state leakage current	V_{EN} = 0 V, VDP/DM_IN = 3.6 V, VDP/DM_OUT = 0 V, measure IDP/DM_OUT			1.5	µA
High-speed data switch - AC parameters(1)						
X_{TALK}	DP, DM crosstalk	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF, V_S = 1 V_{rms}, signal = 0 dBm, f = 250 MHz		47		dB
O_{IRR}	OFF state isolation	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF, V_S = 1 V_{rms}, signal = 0 dBm, f = 250 MHz		17		
B_w	Bandwidth -3 dB	R_{TERM} = 50 Ω, C_{LOAD} = 5 pF, signal = 0 dBm		1100		MHz
Charger emulator - BC1.2 DCP mode						
R_{DCP_RES}	DP_IN to DM_IN short resistance	CTLx configured for DCP BC1.2		100	170	Ω
Charger emulator - divider mode						
V_{DM_1A}	DM_IN output voltage	STCC5011, device set to DCP auto-detect mode or divider mode, V_{IN} = 5.0 V	2.65	2.7	2.75	V
V_{DP_1A}	DP_IN output voltage		1.96	2	2.04	
R_{DM_1A}	DM_IN output resistance	STCC5011, device set to DCP auto-detect mode or divider mode, V_{IN} = 5.0 V		27		kΩ
R_{DP_1A}	DP_IN output resistance			27		
V_{DM_2A}	DM_IN output voltage	STCC5021, device set to DCP auto-detect mode or divider mode, V_{IN} = 5.0 V	1.96	2	2.04	V
V_{DP_2A}	DP_IN output voltage		2.65	2.7	2.75	

Table 4. Electrical characteristics V_{IN} = 4.5 V to 5.5 V, V_{DD} = 1.7 V to 5.5 V, -40 °C < T_J < 125 °C (unless otherwise specified) (continued)

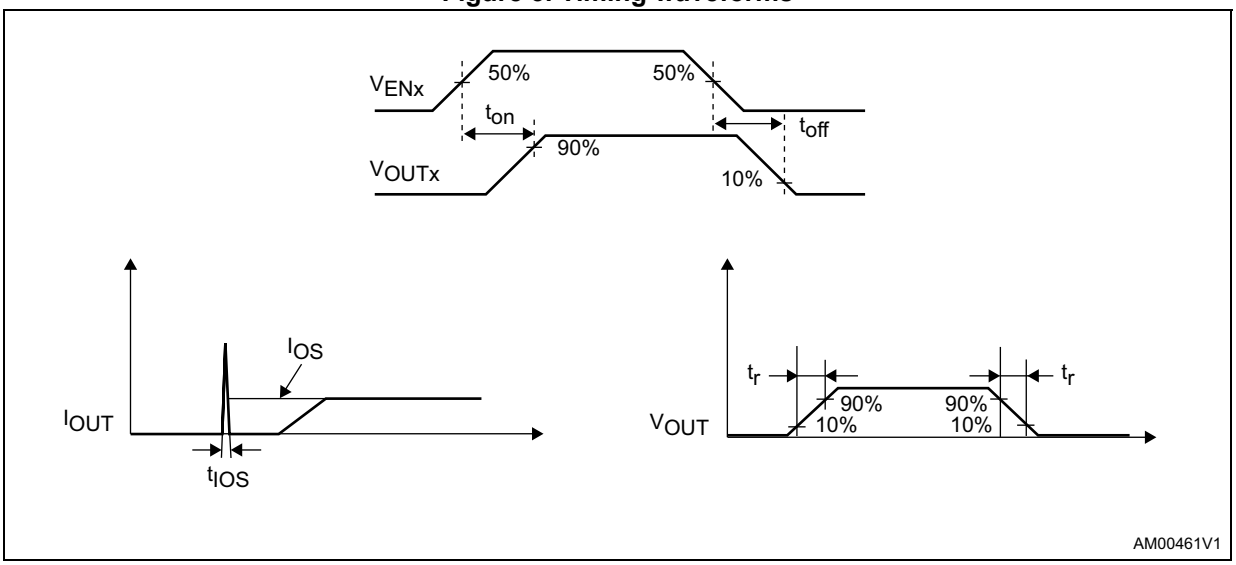
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{DM_2A}	DM_IN output resistance	STCC5021, device set to DCP auto-detect mode or divider mode, V_{IN} = 5.0 V		27		kΩ
R_{DP_2A}	DP_IN output resistance			27		
Charger emulator - BC1.2 CDP mode						
V_{DM_SRC}	Voltage source on DM_IN for CDP detection	V_{DP_IN} = 0.6 V, device in CDP BC1.2 mode	0.5	0.6	0.7	V
V_{DAT_REF}	DP_IN rising voltage threshold to turn on V_{DM_SRC}	I_{DM_IN} = -250 µA, device in CDP BC1.2 mode	0.25	0.32	0.4	
$V_{DAT_REF_HYST}$	V_{DAT_REF} hysteresis			40		mV
V_{LGC_SRC}	DP_IN rising voltage threshold to turn off V_{DM_SRC}		0.8		1	V
$V_{LGC_SRC_HYST}$	V_{LGC_SRC} hysteresis			40		mV
I_{DP_SINK}	DP_IN sink current	0.4 < V_{DP_IN} < 0.8 V, device in CDP BC1.2 mode	50	75	150	µA
Charger emulator - timings						
$t_{CHG_DGL_ON}$	Charging indication ON deglitch delay	From I_{OUT} > I_{OUT_TH} to $\overline{\text{CHARGING/ATTACH}}$ asserted		0.5		s
$t_{CHG_DGL_OFF}$	Charging indication OFF deglitch delay	From I_{OUT} < I_{OUT_TH} to $\overline{\text{CHARGING}}$ deasserted		5		
$t_{VDM_SRC_ON}$	DM_IN voltage source turn-on time	From V_{DP_IN} 0 V -> 0.6 V to V_{DM_IN} = V_{DM_SRC}, CTLx configured for CDP BC1.2		8		ms
$t_{VDM_SRC_OFF}$	DM_IN voltage source turn-off time	From V_{DP_IN} 0.6 V -> 0 V to V_{DM_IN} = 0 V, CTLx configured for CDP BC1.2		1.3		
t_{VBUS_REAPP}	OUT discharge pulse width	From V_{OUT} falling to 0.7 V during discharge to V_{OUT} returning to 90%.	300	350	400	
Charger emulator - control pins CTLx						
V_{CTLx}	CTLx pins threshold voltage		0.4		1.6	V
$V_{HYST(CTLx)}$	Hysteresis voltage on CTLx pins			500		mV
I_{CTLx}	Leakage current	V_{DD} = 5.5 V, V_{IN} = 5.5 V, V_{CTLx} = 0 V or 5 V	-1		1	µA

Table 4. Electrical characteristics V_{IN} = 4.5 V to 5.5 V, V_{DD} = 1.7 V to 5.5 V, -40 °C < T_J < 125 °C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Charger emulator - charging indication						
I_{OUT_TH}	Output current threshold for charging detection	DCP mode, CDP mode		20		mA
$V_{OL(\overline{CHARGING}/\overline{ATTACH})}$	$\overline{CHARGING}/\overline{ATTACH}$ output low voltage	Charging detected (I_{OUT} > I_{OUT_TH}) and charging time in S5 < t_{EOCH} (end of charge safety timer), $I_{\overline{CHARGING}/\overline{ATTACH}}$ = 1 mA			180	mV
$I_{OL(\overline{CHARGING}/\overline{ATTACH})}$	$\overline{CHARGING}/\overline{ATTACH}$ output leakage current	V_{DD} = 5.5 V, V_{IN} = 5.5 V, $V_{\overline{CHARGING}/\overline{ATTACH}}$ = 5 V			1	µA
Charger emulator - safety timer(1)						
t_{EOCH}	Charging timeout after attach detection	From I_{OUT} > I_{OUT_TH} after attach detection to $\overline{CHARGING}/\overline{ATTACH}$ deasserted		3		hours

1. Guaranteed by design. Not tested in production.

Figure 3. Timing waveforms

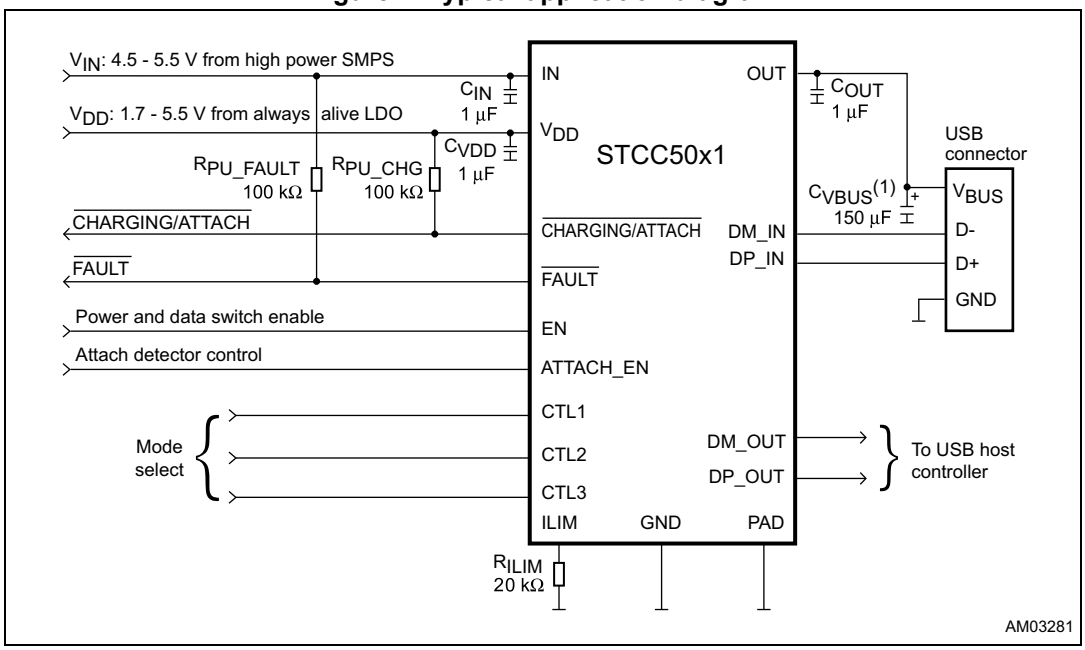


5 Application information

The STCC5011 and STCC5021 devices are designed to be implemented into the PC on a USB port in order to emulate the wall charger adapter when the PC is in standby mode or OFF, and to allow higher charge current when the USB interface is used for data communication. In order to handle these functionalities, the STCC5011/STCC5021 devices rely on USB BC1.2 specifications, Chinese telecommunications industry standard YD/T 1591-2009 and proprietary implementations

- BC1.2 charging profiles are:
  - CDP: charging downstream port providing data communication plus charging (active USB data communications with 1.5 A support)
  - SDP: standard downstream port providing data communication with no charging (active USB 3.0 data communications with 900 mA support or USB 2.0 data communications with 500 mA support)
  - DCP: dedicated charging port (wall charger emulation with no data communication and 500 mA to 1.5 A support)
- Chinese telecommunications standard
  - D+ and D- shorted to allow charging
- Apple divider mode comes in 2 profiles
  - 1 A max. current drawn by Apple iPod, iPhone (STCC5011)
  - 2 A max. current drawn by Apple iPad, supporting also Apple iPod and iPhone (STCC5021)
- BlackBerry emulator mode
- Legacy mode (allowing 500 mA charging current)
- Korean tablet charging mode (D+ and D- shorted and pulled up to a certain voltage)

Figure 4. Typical application diagram



1. C_{VBUS} required by the USB specification.

5.1 Supported modes

For more information refer to *Section 5.4: State machine*.

The STCC5011/STCC5021 device supports the following modes:

- SDP BC1.2
- CDP BC1.2
- SDP with remote wakeup for all USB devices
- CDP with remote wakeup for low-speed USB devices with automatic transition to DCP auto-mode if a full-speed/high-speed USB device attached or after a USB device detached
- DCP auto-detect: this mode permits auto-detection of charging modes between DCP BC1.2 (shorted D+, D-) and divider charging mode. It also supports BlackBerry charging mode and can charge legacy devices and Korean tablets.
- Forced DCP BC1.2 mode
- Forced DCP divider mode

The auto-detect mode starts in divider mode. If a charging negotiation attempt is detected, there is an automatic transition to DCP BC1.2 mode. It is preceded by a V_{BUS} discharge pulse to initialize the proper BC1.2 handshake process. If the BC1.2 device is detached, the circuit automatically returns to divider mode after a 10 s (typ.) timeout.

Note: From the application point of view it means that after removing one device the user should wait for approx. 15 s before attaching another device.

Selection between these modes is made through the CTLx control pins. The CTLx pins may be controlled by the host in different ways:

- GPIO from the embedded controller
- Hardware signals from the USB host controller (SLP_S3#, SLP_S4#) and the AC_adapter signal from the embedded controller
- Hardware signal SUSPEND from the embedded controller and AC_ADAPTER.

Table 5. Truth table control pins CTLx(1)

Host state	CTL1	CTL2	CTL3	Mode description
	0	0	0	Device off, output discharge
S0, S1 (S3)(2)	1	1	0	SDP
S0, S1, (S3)(2)	1	1	1	CDP BC1.2 with charging detection.
S3, (S0, S1)(2)	0	1	0	SDP with remote wakeup for all USB devices
S3	0	1	1	CDP with remote wakeup for low-speed USB devices / DCP auto-mode for full-speed or high-speed USB devices or after a USB device detached.
S4, S5	0	0	1	DCP auto-detect mode without remote wakeup, with charging detection
S4, S5	1	0	1	Forced DCP divider mode with charging detection
S4, S5	1	0	0	Forced DCP BC1.2 mode with charging detection

1. On the transition from the CTLx = 111 to CTLx = 001, a synchronous transition of the CTL1 and CTL2 must be ensured.
2. See *Section 5.2* for further information.

5.2 Remote wakeup in S3

For more information refer to *Section 5.4: State machine*.

If the CTLx pins are controlled by hardware signals (such as SLP_Sx# or SUSPEND), the CTLx combination changes when the host transitions from S0 to S3 and back. In this case, the STCC5011/STCC5021 device can support remote wakeup of portable devices for the following transitions (i.e. no V_{BUS} discharge pulse and data switch ON):

- SDP S0 (CTLx = 110) to and from SDP S3 (CTLx = 010) for all USB devices
- SDP (CTLx = x10) and CDP S0 (CTLx = 111) to and from CDP S3 (CLx = 011) for low-speed USB devices only.

If the host system is in S3 mode (CTLx = 011), the system automatically turns into DCP auto-mode for already attached full-speed / high-speed USB devices or after any USB device is detached. Thus, already attached full-speed / high-speed devices or newly attached devices are charged without the need of CTLx transition.

If the S0 to S3 transition is managed by GPIO from the embedded controller, the easiest solution is to keep the same levels on the CTLx pins (SDP or CDP modes). Therefore, remote wakeup in S3 is supported for all USB devices but the system does not automatically turn into DCP auto-mode.

5.3 V_{BUS} discharge

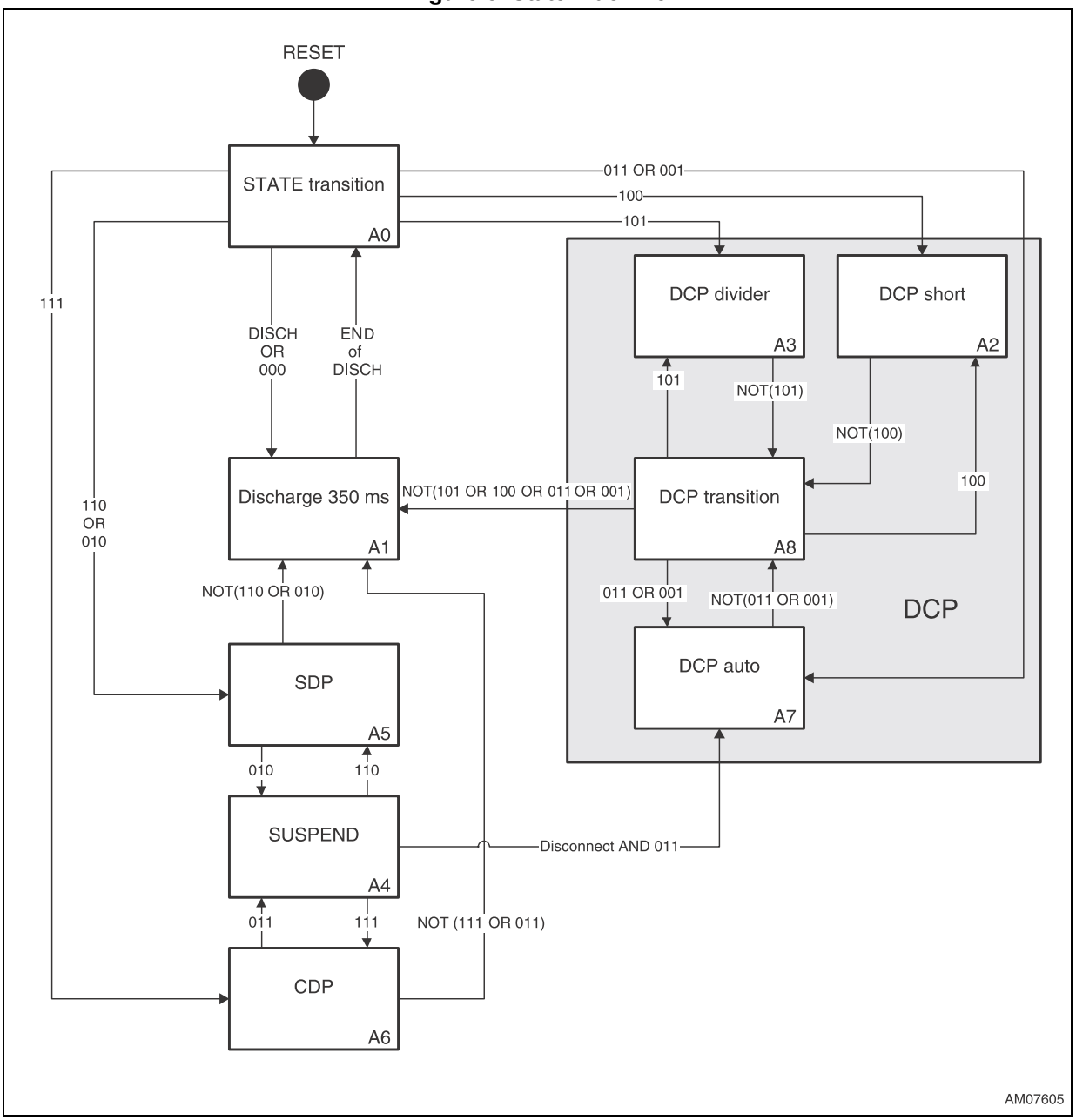
The V_{BUS} discharge pulse lasts for 350 ms typ. (t_{VBUS_REAPP}) and is performed for any transitions between the modes listed in *Table 5*, except the modes allowing remote wakeup in S3 [transitions (x10) and (111) to/from (011)].

Permanent output discharge is provided in the following modes:

- EN = 0, ATTACH_EN = 0, CTLx = xxx (ignored)
- EN = 1, ATTACH_EN = 0, CTLx = 000.

5.4 State machine

Figure 5. State machine



5.5 Attach detection

The STCC5011-STCC5021 can detect peripheral device attachments when the host system is in S4/S5 deep sleep states or in G3 shutdown state.

In these states, when no peripheral device is attached, the host system can save power by switching off the high-power DC-DC converter and switching on a low-power LDO on the IN pin of the device. When an attach event is detected, the device asserts the $\overline{\text{CHARGING/ATTACH}}$ output allowing the host system to turn off the low power LDO and turn on the high power DC-DC converter and start charging.

The attach detection feature is enabled with the combination of logic low level on EN and logic high on ATTACH_EN (see *Table 6*). The devices already attached when activating the attach detection circuit (EN = 0, ATTACH_EN = 1) are ignored and their current consumption is limited to 500 µA. Only devices attached after activation of the attach detection circuit are detected.

Table 6. Attach detector truth table

ATTACH_EN	EN	Attach detector
0	x	OFF
1	1	OFF
1	0	ON

The attach detection block is supplied by the V_{DD} power supply pin. It has a very low consumption (12 µA typ.) and accepts a wide supply voltage range (1.7 V up to 5.5 V). The V_{DD} power supply must be provided by a dedicated low power LDO.

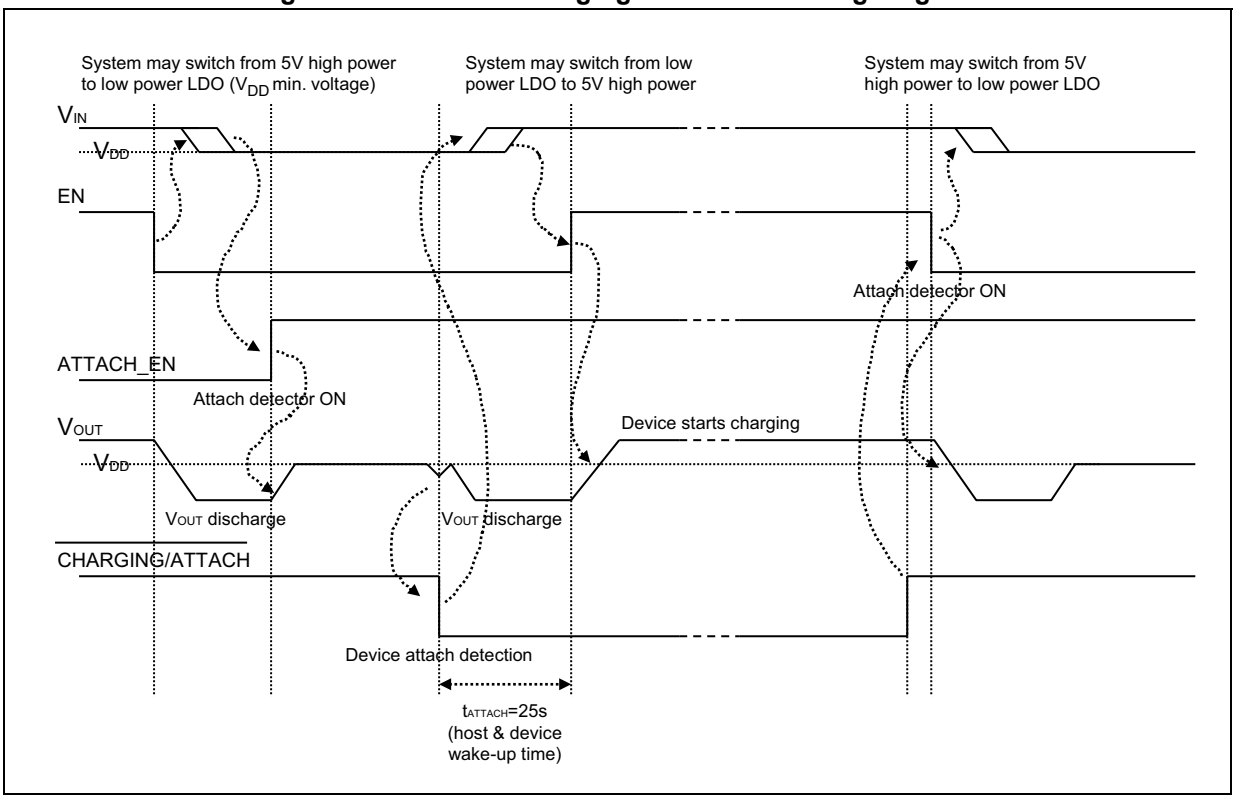
The attach detector monitors voltage drop across a bypass switch between V_{DD} and the OUT pin. The bypass switch is enabled only when the attach detector is turned on. This voltage drop is caused either by the supply current of the attached device or by inrush current for charging device internal capacitors.

The open drain active low output $\overline{\text{CHARGING}}/\overline{\text{ATTACH}}$ is asserted upon device detection, alerting the host system of device attachment. It stays asserted for the t_{ATTACH} delay (25 s typically). During this time, the host system may switch the IN pin from low power LDO to 5 V high-power supply and set proper CTLx configuration (see *Figure 6*).

The attached device can start charging keeping $\overline{\text{CHARGING}}/\overline{\text{ATTACH}}$ asserted. If charging does not occur, the flag is deasserted after the t_{ATTACH} (the attached device removed or charging current drops below threshold or safety timer expires - see *Section 5.6*).

The supply voltage of the low-power LDO connected to the IN pin, when the system is in power saving mode, must not be lower than the V_{DD} power supply voltage level and must not be greater than 5.5 V.

Figure 6. Attach and charging detection - Timing diagram



5.6 Charging detection and safety timer

The STCC5011-STCC5021 devices continuously monitor current drawn by the portable device. While programmed in CDP or DCP mode, the STCC5011-STCC5021 devices send a charging flag to the system if the current through the USB power switch is above the charging threshold, set at 20 mA typ.: open drain active low output $\overline{\text{CHARGING/ATTACH}}$ is asserted.

Note: In CDP mode the charging flag is asserted only if the CDP handshaking between the portable device and the host is performed before the current is above threshold.

If the $\overline{\text{CHARGING/ATTACH}}$ output is already asserted because of attachment detection (while the host is in S4/S5 states or G3 state), this output stays unchanged.

For systems in S5 providing current charge while being battery supplied, there is a safety timer integrated into the STCC5011-STCC5021 devices. This timer is started only after an attach event with input ATTACH_EN enabled.

The safety timer is stopped in the following conditions:

- Charging current below threshold (see *Figure 7*). The $\overline{\text{CHARGING/ATTACH}}$ output is deasserted.
- End of 3 hours (timer expires). The $\overline{\text{CHARGING/ATTACH}}$ output is deasserted.
- ATTACH_EN transition to 0 (see *Figure 8*). The $\overline{\text{CHARGING/ATTACH}}$ output is intact and the charging can continue without any time limit.

Figure 7. 3-hour timer - start and stop

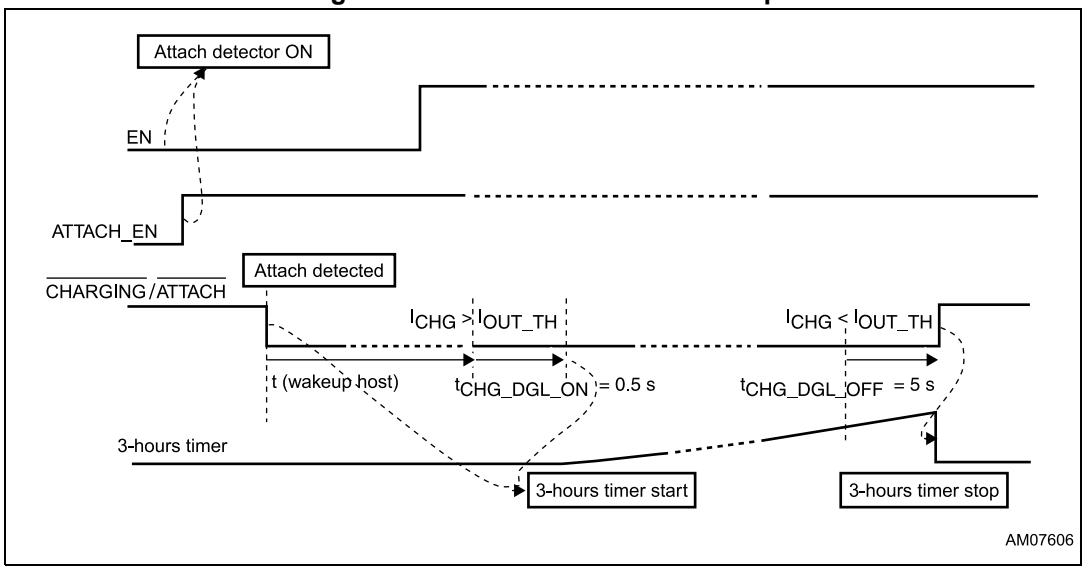
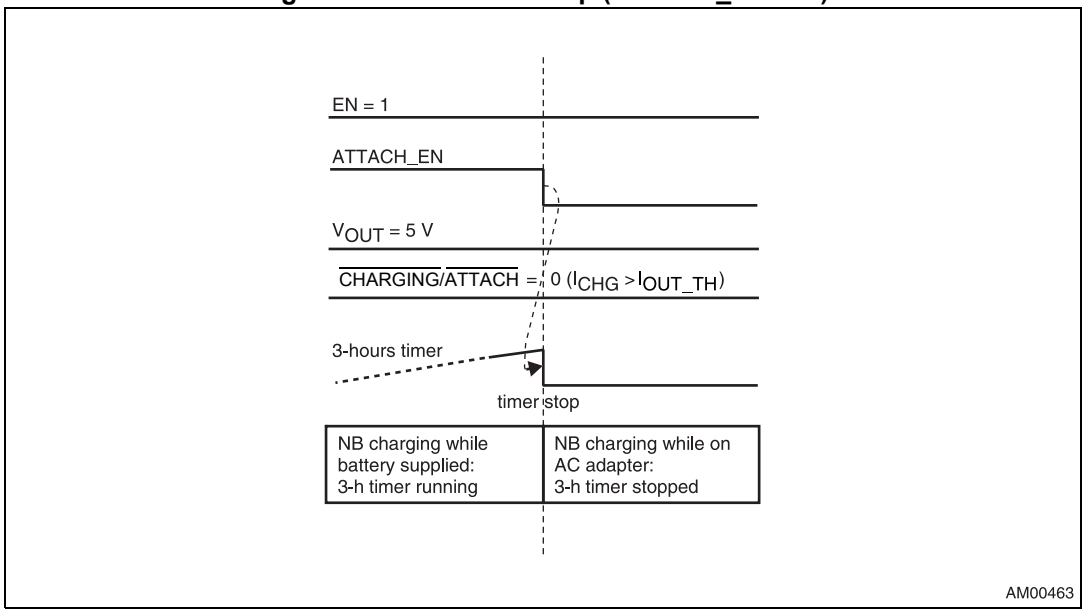


Figure 8. 3-hour timer stop (ATTACH_EN low)



Use case 1: device charging in CDP, notebook is then turned off

If a device is charging while the system is turned off and the battery supplied, the risk is that the charging process stops before the end of charge due to the system power-off. To avoid this, the flag CHARGING/ATTACH can be used by the host to prevent the switching-off of the high power DC-DC converter when the host goes to S5 state, even if battery supplied. In this case the 3-h timer is not started.

Use case 2: charging in S5, battery supplied

Once device attachment has been detected and the host has woken up, supplying V_{BUS} voltage to the portable device allows the charging process to start in DCP mode. The flag CHARGING/ATTACH stays asserted for the t_{ATTACH} period (25 s typ.) after attach. During this period, the charging must be established (charging current above the I_{OUT_TH} threshold) to keep the CHARGING/ATTACH output asserted. The 3-h safety timer is started if ATTACH_EN is kept high.

If, for whatever reason, there is no charging current (or if it is below 20 mA), CHARGING/ATTACH is deasserted (while ATTACH_EN is still high). The host can return to its previous state by switching off the high power supply and switching on the low-power LDO, to reduce consumption, and setting the EN pin to 0. Therefore, the attach detector is ON. At this stage, the STCC5011-STCC5021 devices can detect if the device is still attached or has been removed (see *Figure 9*).

- If the device is still attached, the attach detector circuit waits for device removal.
- If the device is removed, the circuit goes back into attach detection mode till the next attachment.

Figure 9. Attach detection

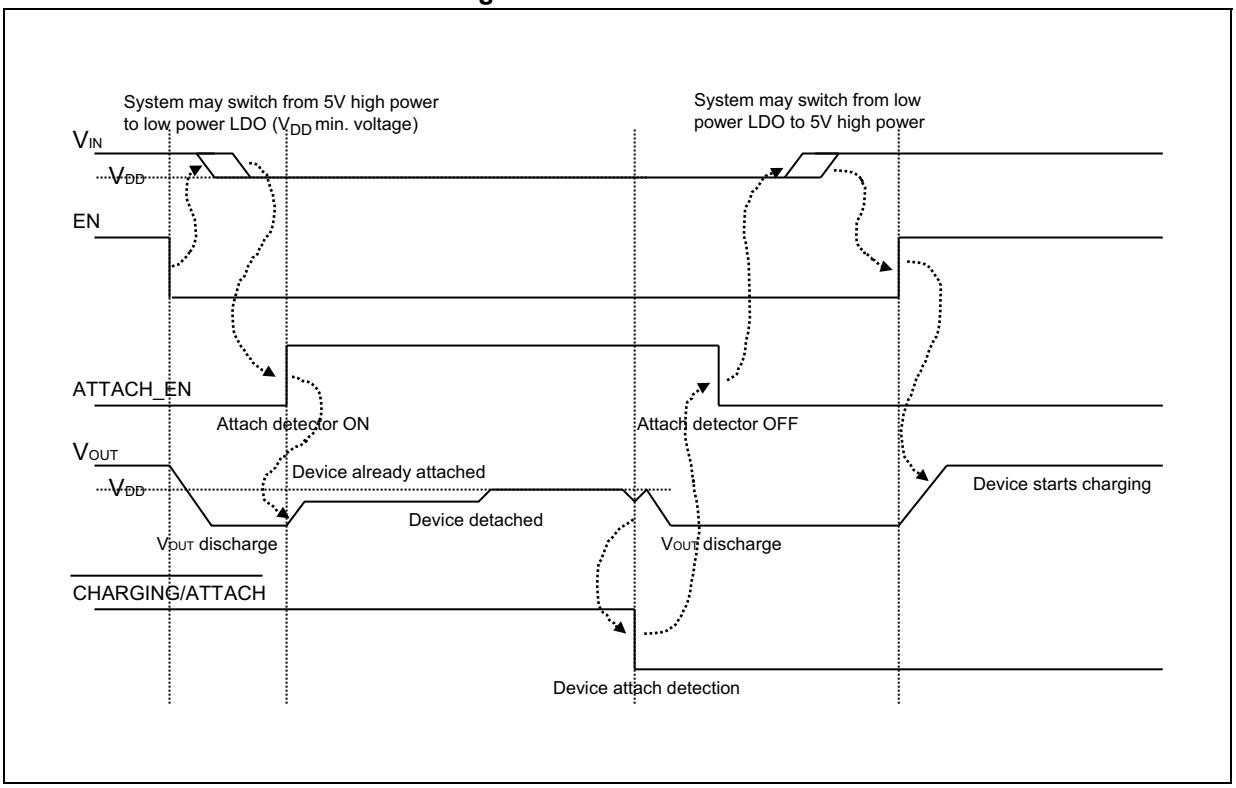
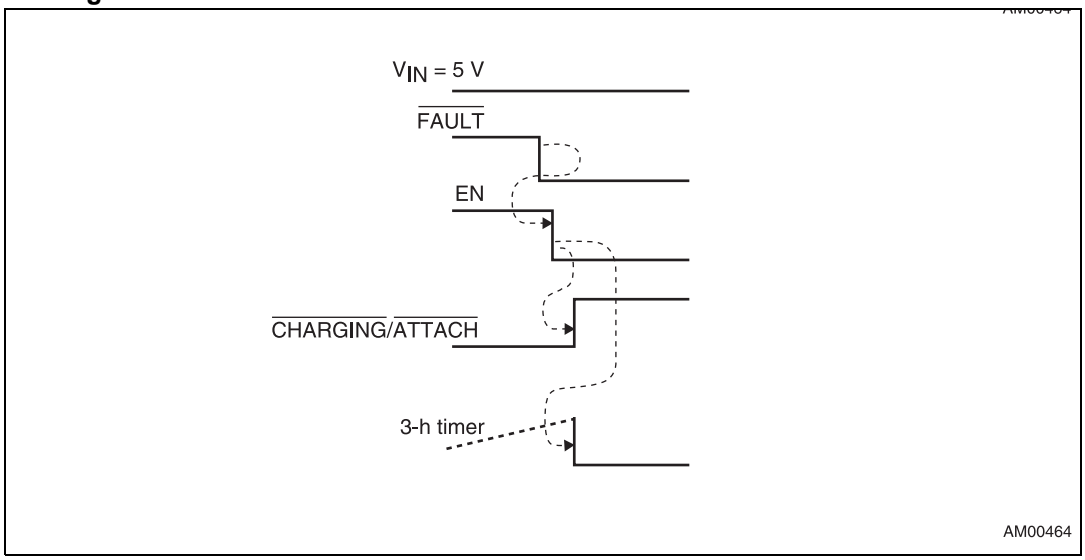


Figure 10. Reset of $\overline{\text{CHARGING}}/\overline{\text{ATTACH}}$ and 3-hour timer after EN -> 0 event



5.7 Power switch

Overcurrent conditions

When an overcurrent condition is detected, the device maintains a constant output current and reduces the voltage accordingly. There are two overload conditions:

- The first one occurs when a short-circuit or a partial short-circuit is already present when the device is being powered up or enabled. The output voltage is held near zero potential with respect to ground and the STCC50x1 device ramps the output current to I_{OS} until the overload condition is removed or the device starts thermal cycle.
- The second condition is when a short-circuit, a partial short-circuit, or a transient overload occurs while the device is already enabled and powered-on. The STCC50x1 device responds to the overcurrent condition within time t_{IOS}. The current sense amplifier is overdriven during this time and momentarily disables the internal current limit MOSFET. It then recovers and ramps the output current to I_{OS}. Similar to the previous condition, it limits output current to I_{OS} until the overload condition is removed or thermal cycle starts.

Thermal protection

The STCC50x1 devices have an internal thermal sensing circuit which monitors the operating temperature of the circuit. It disables power switch operation if die temperature exceeds temperature threshold T_{STOP}, set at 150 °C. The thermal sensor has a hysteresis of 20 °C. The switch turns on if the temperature has cooled down by 20 °C.

Undervoltage lockout

The UVLO circuit disables the circuit until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop during turn-on.

$\overline{\text{FAULT}}$ functionality

The $\overline{\text{FAULT}}$ open drain active low output is asserted during overcurrent or overtemperature conditions. Signal is asserted until the fault is removed.

For overcurrent conditions, the STCC50x1 device is designed to eliminate false $\overline{\text{FAULT}}$ reporting, by using an internal deglitch delay (9 ms typ.).

In the case of overtemperature, there is no deglitch delay and the $\overline{\text{FAULT}}$ signal is asserted immediately. It is deasserted with delay after the device has cooled down and begins to turn on. This unidirectional glitch immunity prevents $\overline{\text{FAULT}}$ oscillation during an overtemperature event.

In the case of fault condition, the host may disable the power switch by toggling EN input to logic low (see *Figure 10*).

Current limit programming

Current limit can be adjusted by an external resistor in the range 500 mA to 2.8 A (typ.). The programming resistor may be calculated using *Equation 1* to *Equation 3*:

Equation 1

$$I_{OS(typ)} = \frac{48000}{R_{ILIM}} (\text{mA, k}\Omega)$$

Equation 2

$$I_{OS(min)} = \frac{48000}{R_{ILIM}^{1.037}} (\text{mA, k}\Omega)$$

Equation 3

$$I_{OS(max)} = \frac{48000}{R_{ILIM}^{0.962}} (\text{mA, k}\Omega)$$

Equation 2 and *Equation 3* allow the minimum and maximum variation to be estimated around the typical value predefined by the external resistor, R_{ILIM}, given in *Equation 1*.

Equation 2 and *Equation 3* do not take into consideration external resistor variations.

5.8 EN functionality

The enable input (EN, active high) serves to turn off the STCC50x1 device and achieve the lowest current consumption.

The behavior of the STCC50x1 device in disabled state (EN = 0) is as follows:

- Power switch, USB data switch and emulation profiles are turned off
- The $\overline{\text{FAULT}}$ and $\overline{\text{CHARGING}}/\overline{\text{ATTACH}}$ flags are cleared (the $\overline{\text{FAULT}}$ and $\overline{\text{CHARGING}}/\overline{\text{ATTACH}}$ outputs are set to Hi-Z mode)
- If ATTACH_EN = 0, permanent output discharge is turned on
- If ATTACH_EN = 1, the device turns into the attach detection mode.

5.9 Input and output capacitors

For proper functionality the STCC50x1 device requires 1 µF decoupling ceramic capacitors C_{IN}, C_{VDD} and C_{OUT} (see *Figure 4*). These capacitors should be placed as close as possible to the corresponding pins.

The electrolytic capacitor C_{VBUS} (see *Figure 4*) is required by the USB specification to suppress the voltage and current transients caused by hot plugging/unplugging the peripheral devices. This capacitor should be placed as close as possible to the USB connector. The recommended value is 150 µF, low ESR type is preferred.

If the V_{IN} supply path is longer than approx. 150 mm, an additional capacitor is required to be connected in parallel to the C_{IN} to suppress V_{IN} overvoltage transients caused by supply path inductance and fast current changes. The minimum value is 10 µF, low ESR type is preferred.

6 Typical operating characteristics

Figure 11. Power switch ON resistance vs. temperature

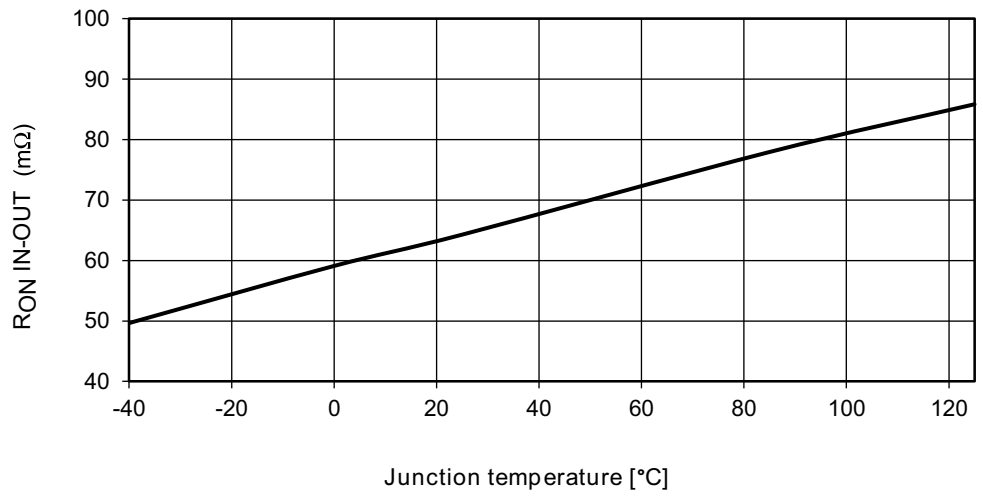


Figure 12. OUT discharge resistance vs. temperature

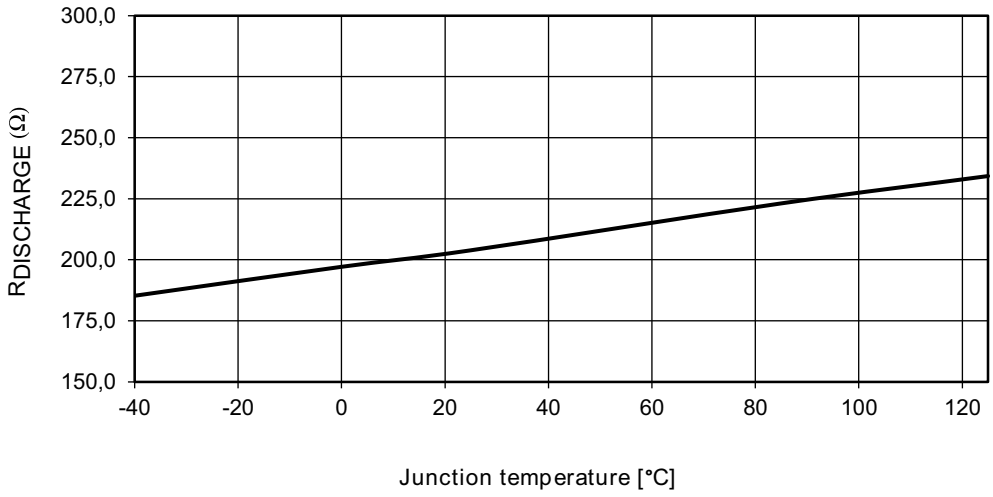


Figure 13. OUT short-circuit current limit vs. temperature (R_{ILIM} = 96 kΩ)

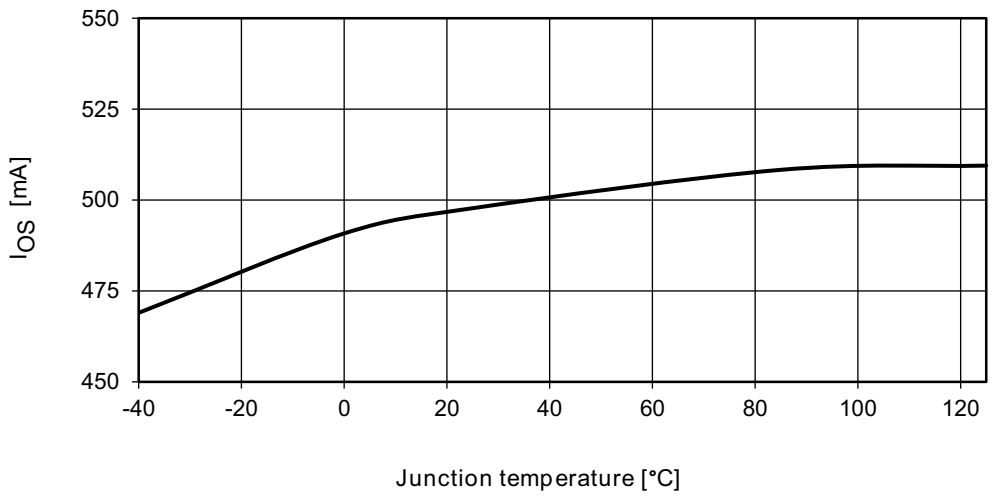


Figure 14. OUT short-circuit current limit vs. temperature (R_{ILIM} = 33 kΩ)

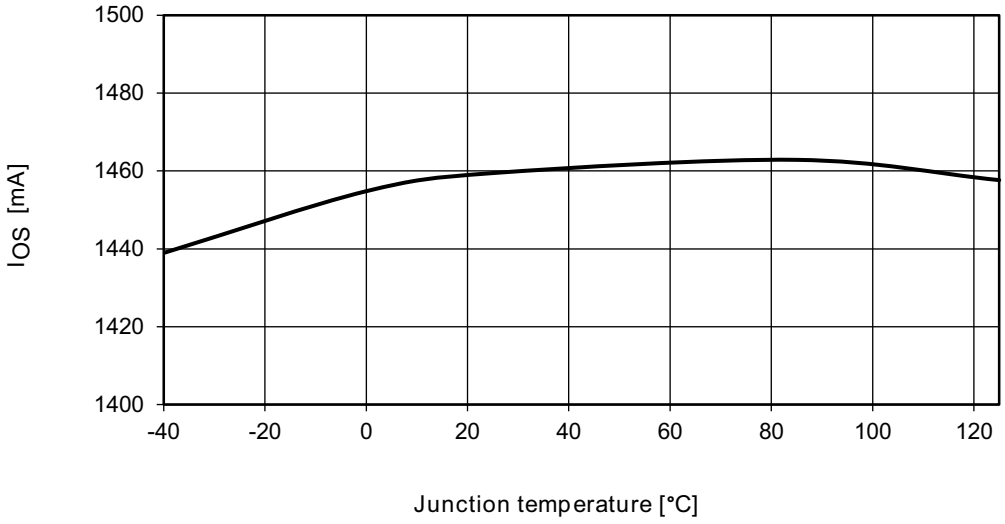


Figure 15. OUT short-circuit current limit vs. temperature (R_{ILIM} = 19.6 kΩ)

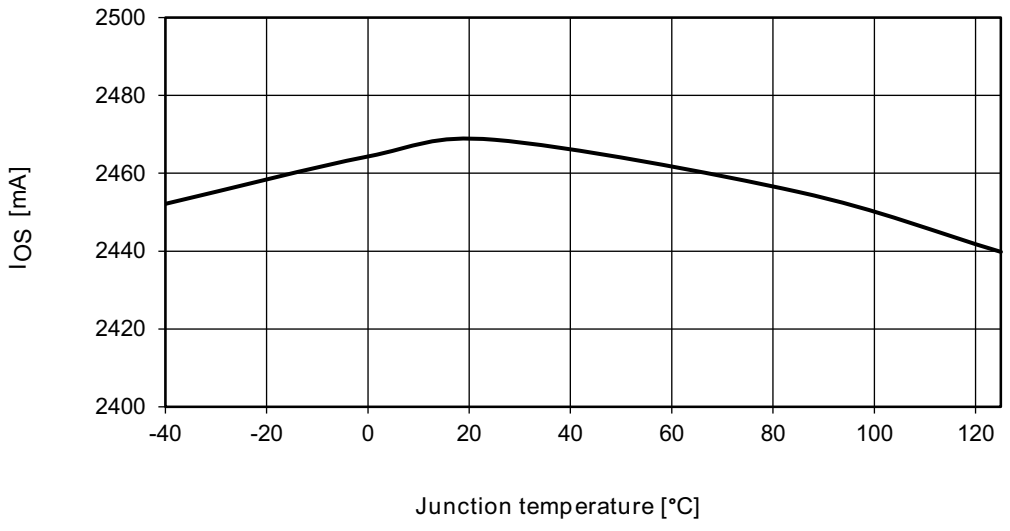


Figure 16. Disabled IN supply current vs. temperature

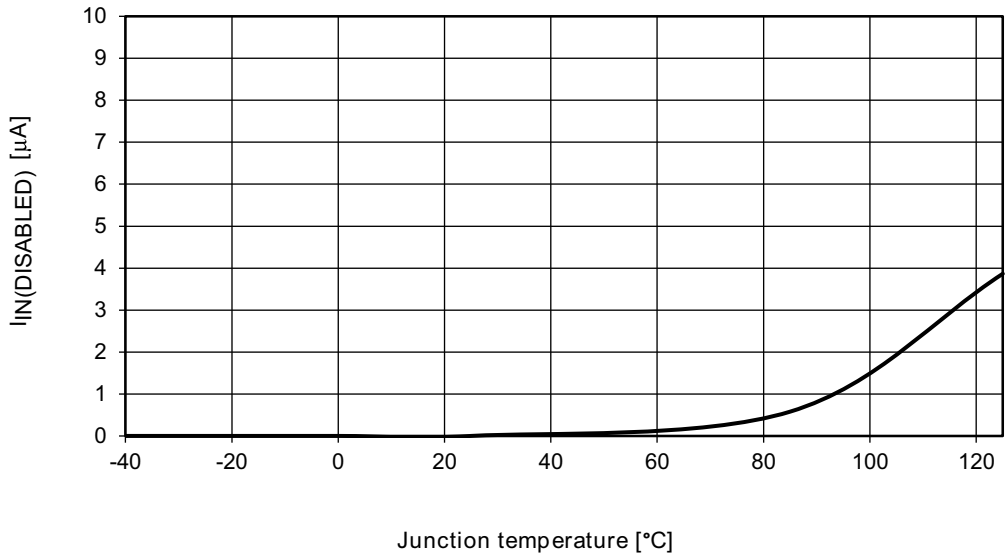


Figure 17. Enabled IN supply current vs. temperature (SDP mode)

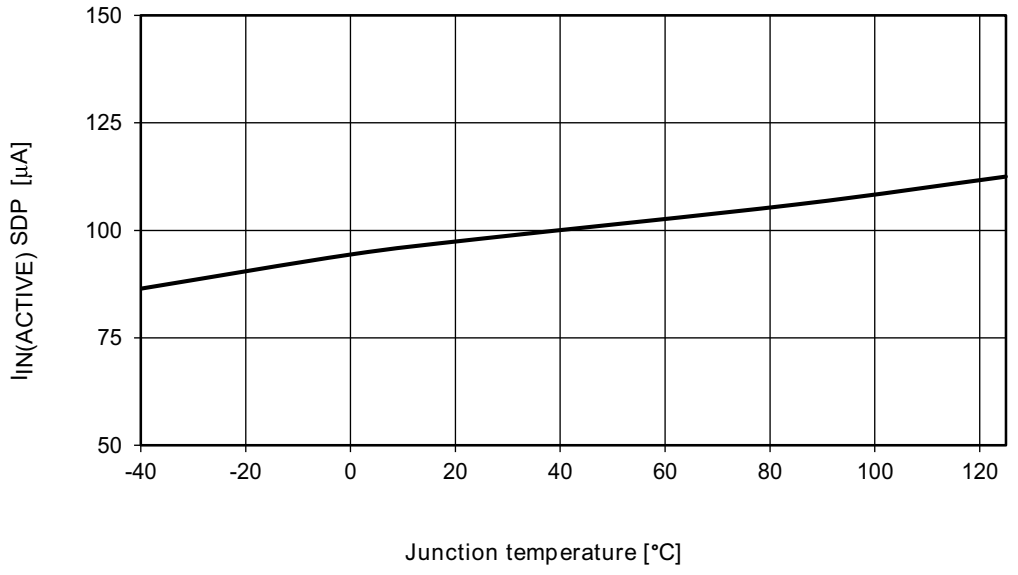


Figure 18. Enabled IN supply current vs. temperature (CDP mode)

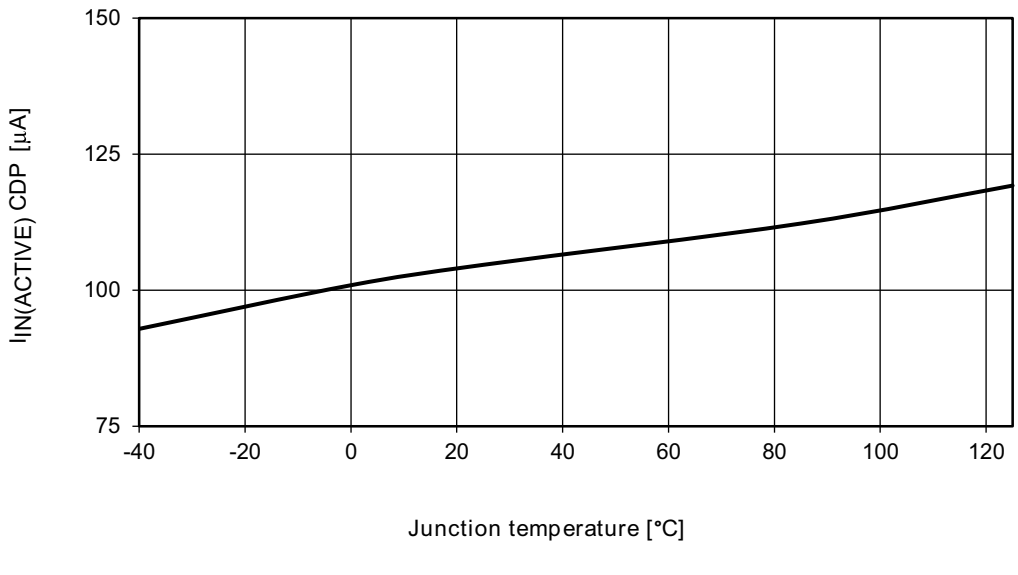


Figure 19. Enabled IN supply current vs. temperature (DCP auto-mode)

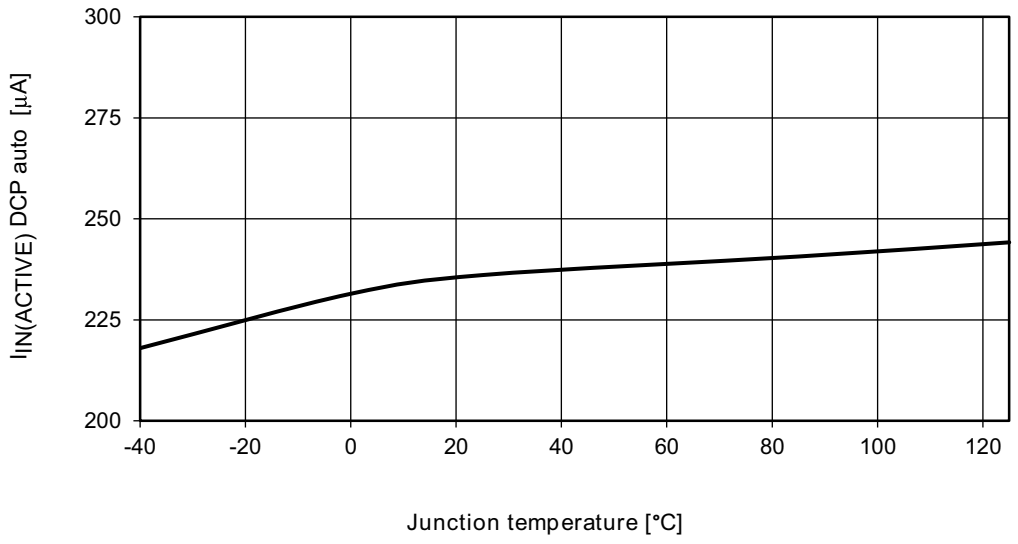


Figure 20. Enabled IN supply current vs. temperature (DCP BC1.2 mode)

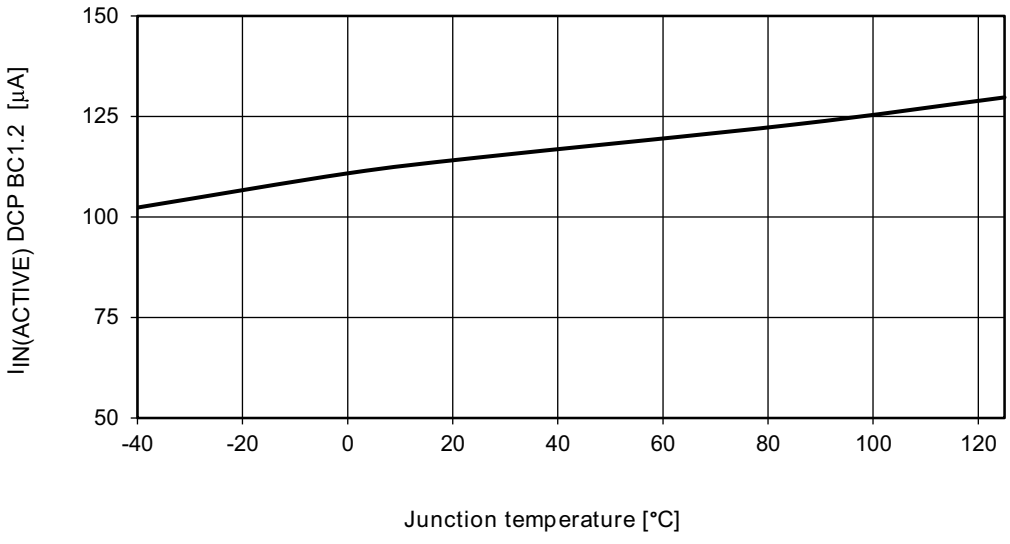


Figure 21. Enabled IN supply current vs. temperature (DCP divider mode)

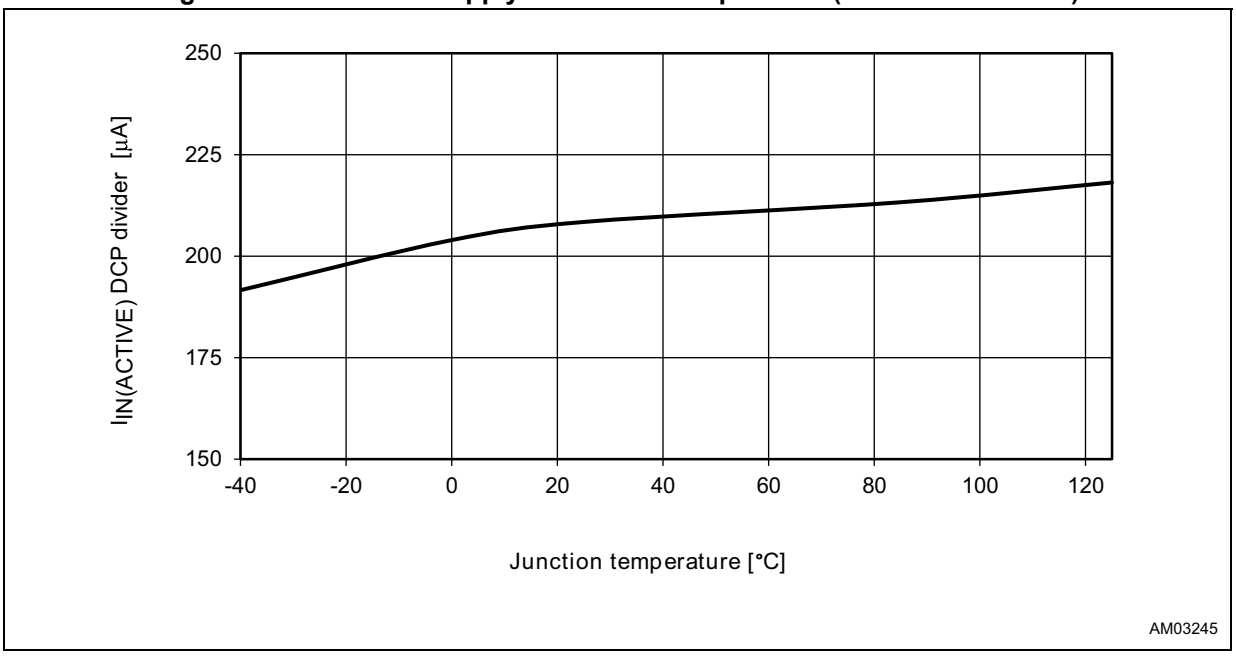


Figure 22. Data switch transfer characteristics vs. frequency

Figure 23. Eye diagram using USB compliance test pattern - without STCC50x1 (deskew line + cable)

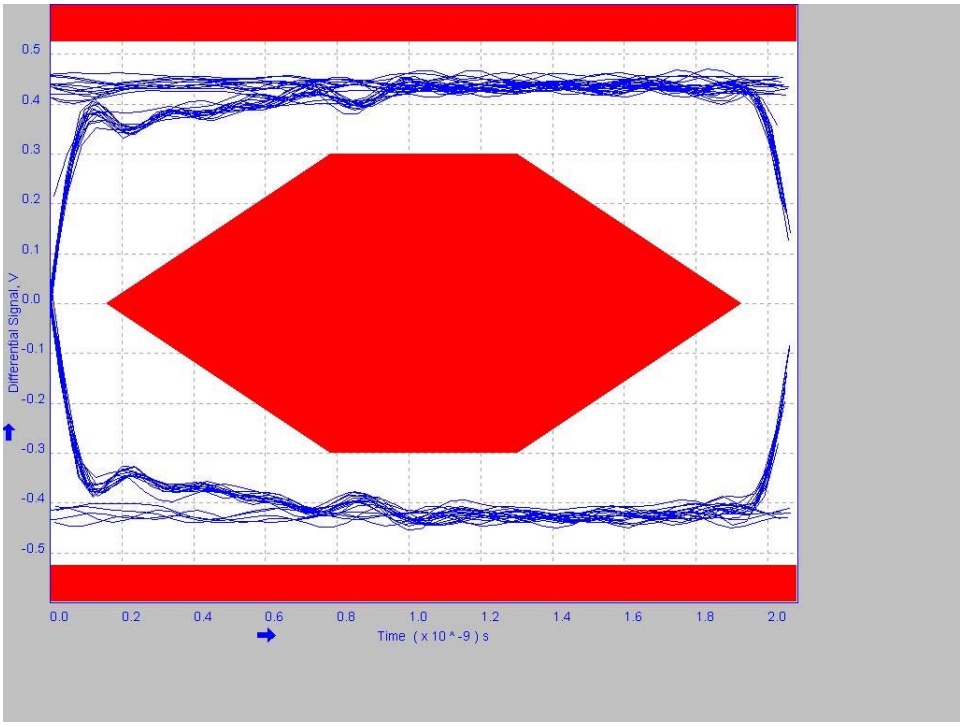


Figure 24. Eye diagram using USB compliance test pattern - with STCC50x1 (STCC50x1 + cable)

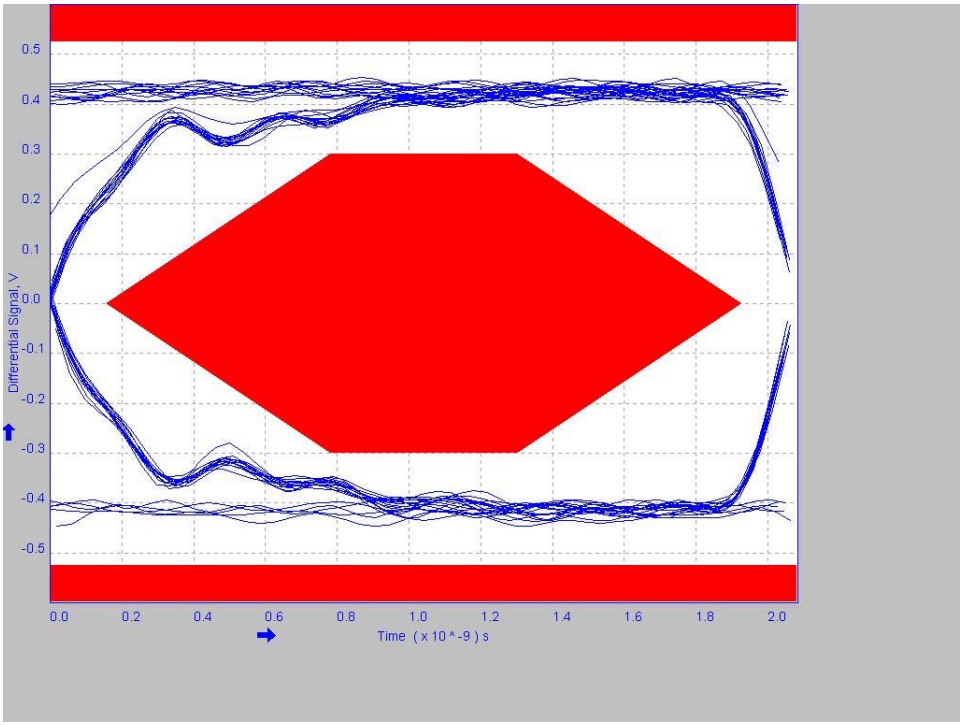


Figure 25. Turn-on response (R_{ILIM} = 20 kΩ, R_{LOAD} = 5 Ω, C_{LOAD} = 150 µF)

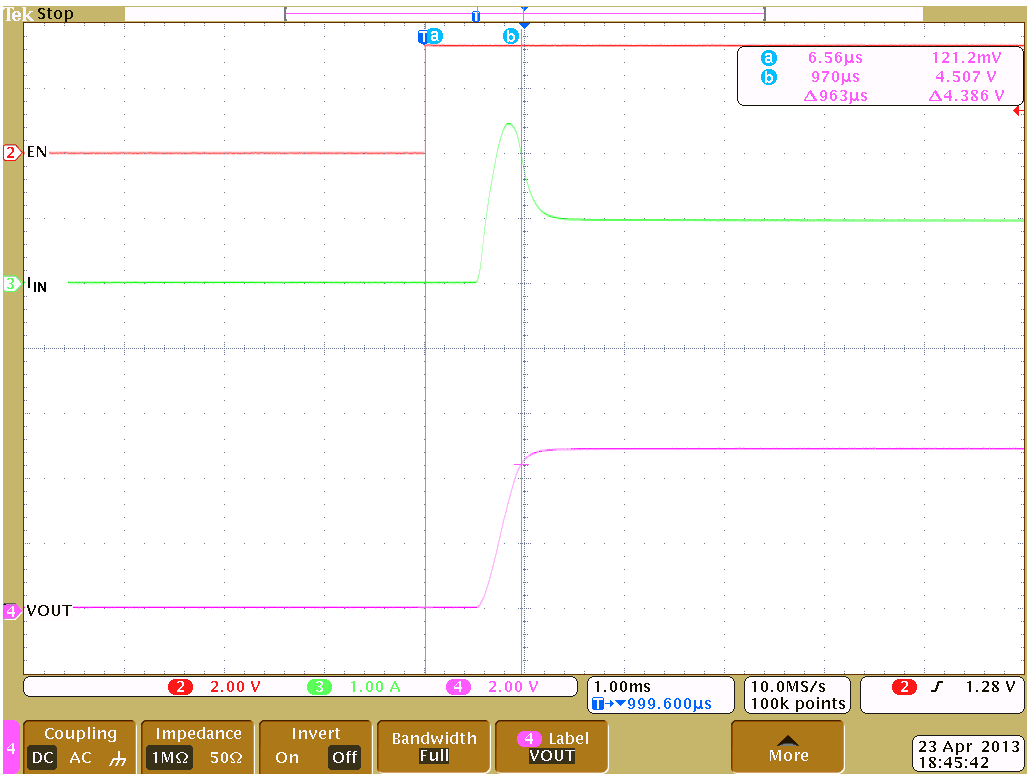


Figure 26. Turn-off response (R_{LOAD} = 5 Ω, C_{LOAD} = 150 µF)

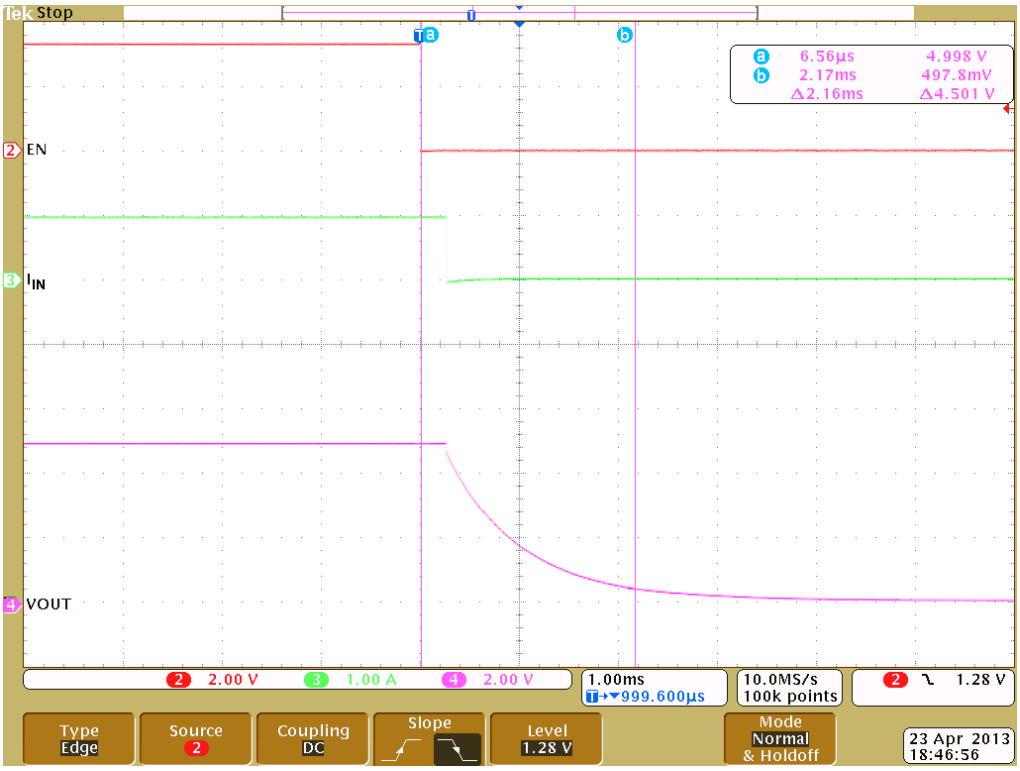


Figure 27. Device enabled into short-circuit (R_{ILIM} = 80.6 kΩ)

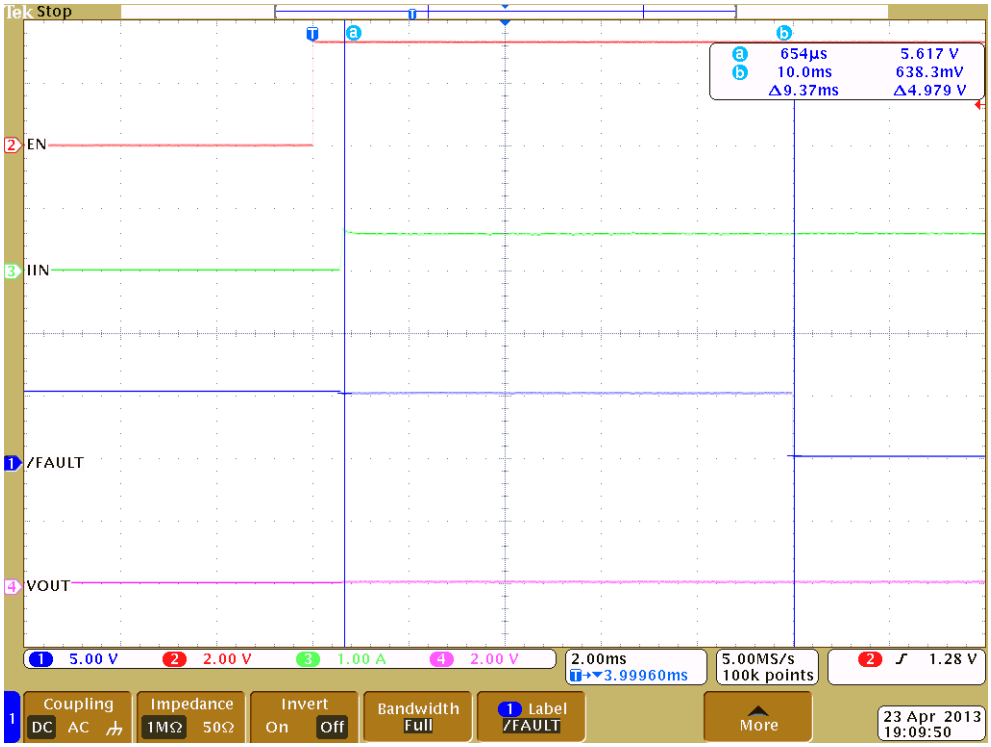


Figure 28. Device enabled into short-circuit - thermal cycling (R_{ILIM} = 20 kΩ)

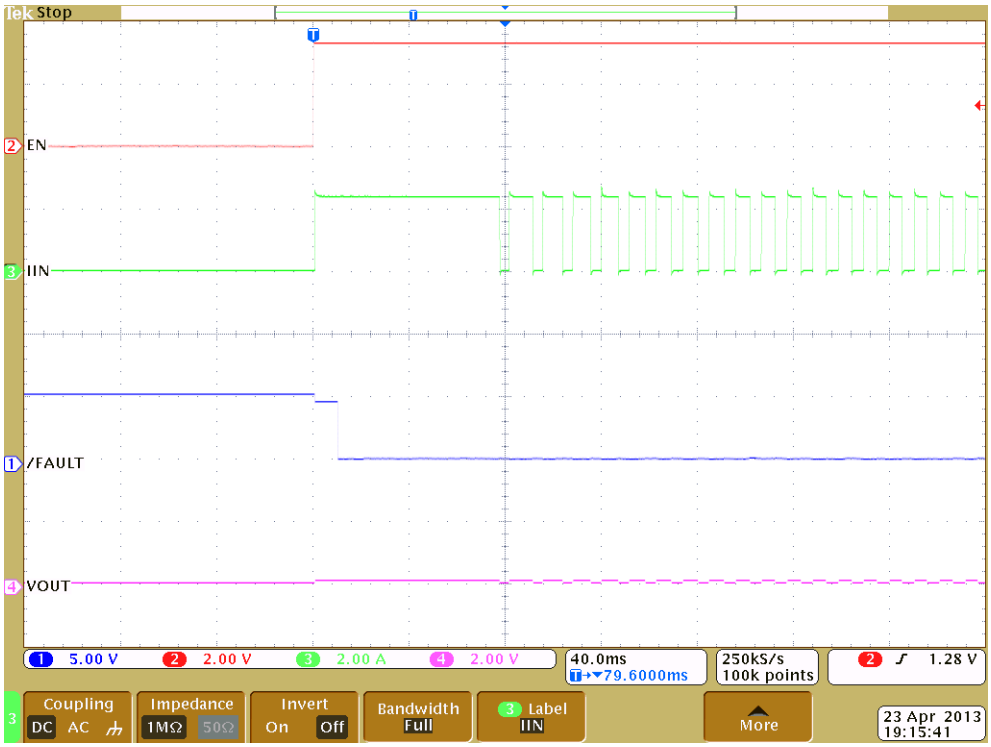
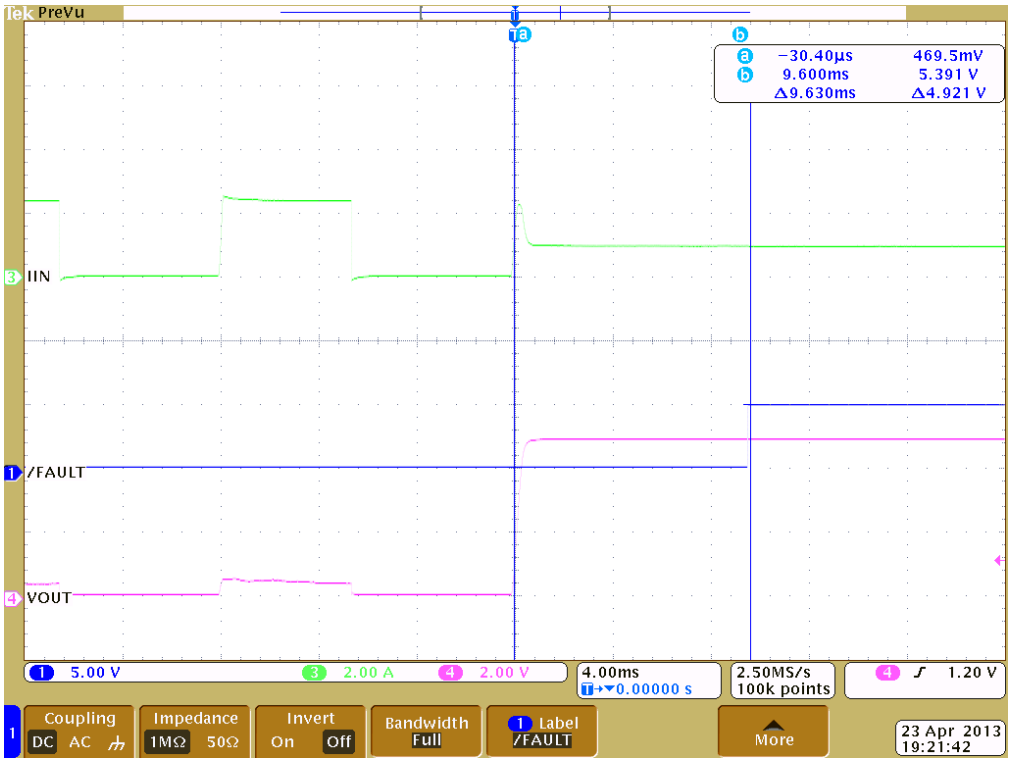


Figure 29. Short-circuit to full load recovery (R_{ILIM} = 20 kΩ, R_{LOAD} = 5 Ω, C_{LOAD} = 150 µF)



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 30. VFQFPN 16L - 3 x 3 x 0.8 mm with exposed pad 1.7 - package outline

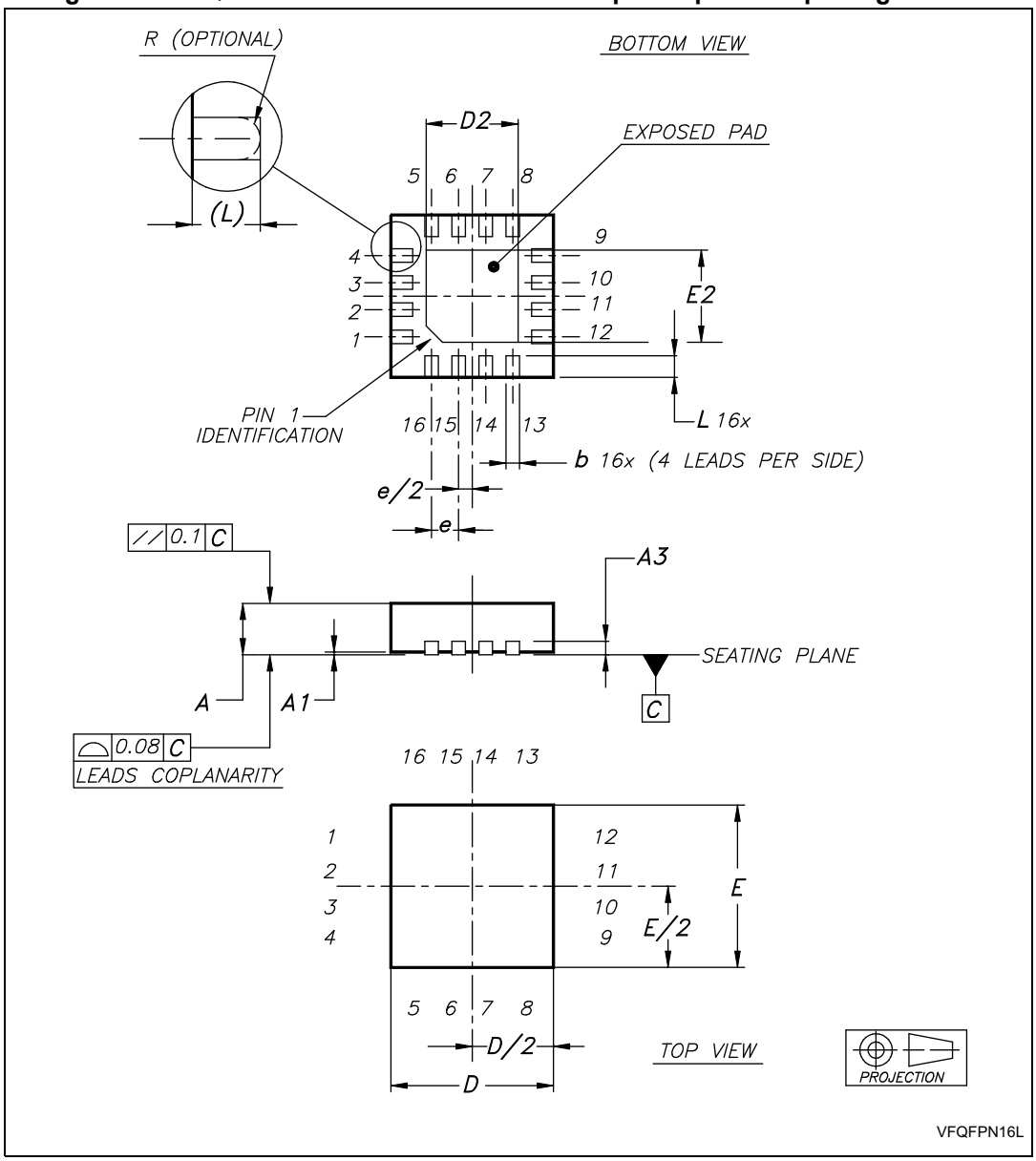
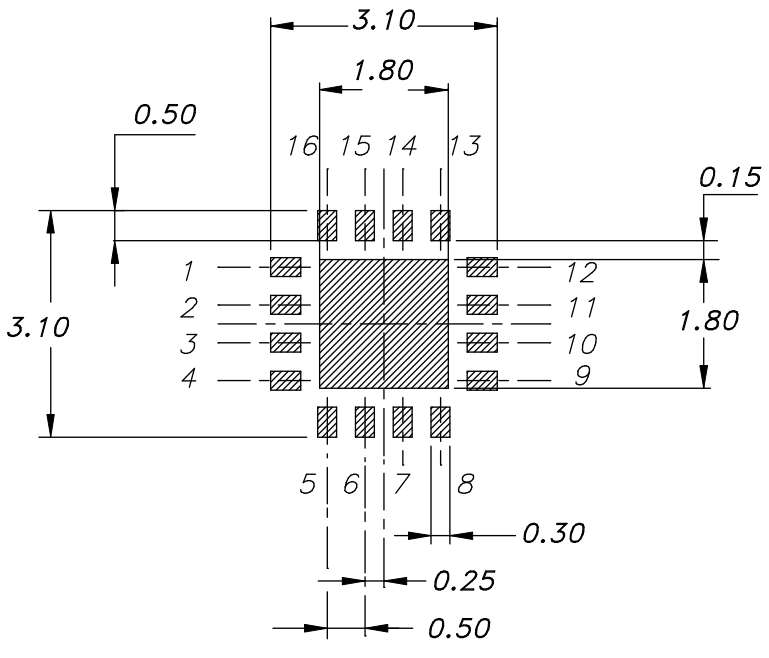


Table 7. VFQFPN 16L - 3 x 3 x 0.8 mm with exposed pad 1.7 - package mechanical data(1), (2), (3), (4)

Symbol	Dimensions			Notes
	Data book (mm)			
	Nom.	Min.	Max.	
A	0.75	0.70	0.80	
A1	0.02	0	0.05	
A3	0.20			
b	0.25	0.18	0.30	
D	3	2.90	3.10	
D2	1.70	1.50	1.80	
E	3	2.90	3.10	
E2	1.70	1.50	1.80	
e	0.50			
L	0.40	0.30	0.50	(5)

1. VFQFPN - standard for “thermally enhanced very thin fine pitch quad flat package no leads”.
2. The lead size is comprehensive of the thickness of the lead finishing material.
3. Dimensions do not include mold protrusion, not to exceed 0.15 mm.
4. Package outline exclusive of metal burr dimensions.
5. The value of “L” a JEDEC norm is min. 0.35 – max. 0.45.

Figure 31. VFQFPN 16L - 3 x 3 x 0.8 mm with exposed pad 1.7 - recommended footprint



8 Ordering information

Table 8. Order codes

Order code	Apple divider mode	Temperature range	Marking	Package	Packaging
STCC5011IQTR	1 A	-40 to 85 °C	5011CC	VFQFPN 16L	Tape and reel
STCC5021IQTR	2 A		5021CC		

9 Revision history

Table 9. Document revision history

Date	Revision	Changes
20-May-2013	1	Initial release.
24-Jun-2013	2	Updated *Features on page 1* (added UL and CB recognized components). Updated note *3.* below *Table 2* (updated data, added cross-reference to *Figure 4*). Updated *Table 4* (updated parameters and conditions to $\lvert I_{REVERSE} \rvert$, $I_{OL(\overline{FAULT})}$, $I_{OL(\overline{CHARGING}/\overline{ATTACH})}$, I_{CTLx}, $I_{OL(\overline{CHARGING}/\overline{ATTACH})}$ symbols, added I_{ATTACH_EN} symbol). Added *Figure 4 on page 12*. Added *Note:* in *Section 5.1 on page 13*. Added *Section 5.9 on page 22*.
06-Dec-2013	3	Updated *Table 4* (updated min. conditions for I_{OS} - R_{ILIM} 96 kΩ and R_{ILIM} 33 kΩ). Updated *Table 5* (updated Host state column, added footnote *1.* and *2.*below table). Updated *Section 5.7* (replaced equation by *Equation 1* to *Equation 3*). Minor modifications throughout document.
06-Feb-2014	4	Replaced adjustable current limit with 2.8 A throughout document *Table 4*: added current limiter threshold condition “R_{ILIM} = 17.2 kΩ"
25-Feb-2014	5	*Section 5.7: Power switch*: updated *Equation 2* and *Equation 3* and added explanation of same. *Table 8: Order codes*: added “Marking”
26-Aug-2014	6	*Description*: added information about S4/S5 deep sleep off states and G3 shutdown state. *Section 5.5: Attach detection*: added information about S4/S5 deep sleep off states and G3 shutdown state; replaced *Figure 6*. *Section 5.6: Charging detection and safety timer*: updated text with respect to S4/S5 states and switching on the low-power LDO; replaced *Figure 9*.

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